Designing With Foil Resistors in Hermetic Packages
(The ultimate in resistor network performance)

When relative performance along with absolute performance is a resistance requirement, the preferred solution is a network of resistors. The combining of resistors in a common package reduces the temperature variation by sharing the heat during non-uniform loading. Table 1 shows the expected performance from resistor networks made in various ways, including thick film, thin film, and Bulk Metal® foil. The following discussion elaborates on the expected performance improvements when moving up the technology ladder to the foil network in a hermetic enclosure.

TABLE 1 - NETWORK PERFORMANCE

NETWORK TECHNOLOGY	THICK FILM	THIN FILM	HERMETIC FOIL
Absolute tolerance	1 %	0.10 %	0.005 %
Ratio tolerance available	1 %	0.10 %	0.005 %
Temperature coefficient	300 ppm/°C	25 ppm/°C	5 ppm/°C
TCR tracking	100 ppm/°C	10 ppm/°C	0.5 ppm/°C
Tracking change with load life	500 ppm	250 ppm	20 ppm
Δratio with moisture	1000 ppm	5000 ppm	10 ppm
Rise time	50 ns	10 ns	1 ns without ringing
Resistance to soldering heat	0.25 % - 3 %	0.10 %	0.01 %

The Underlying Technologies

Foil Resistors are made by rolling a nickel/chromium alloy down to a 100 µin thickness and bonding it to a ceramic substrate. A selection of masks permits value determination followed by binning and subsequent calibration. There are normally no NRE charges because the parts are individually drawn from an established inventory of chips. Further improvement is possible by having two or more values sharing the same substrate and by applying post-manufacturing operations.

Thin Film Resistors are made by depositing a resistive alloy onto a ceramic surface. The deposition layer is about 250 Å thick and requires careful masking to create the network image for subsequent calibration. This masking is also subject to an NRE charge for any values which are not part of the standard production line, and can result in long lead times.

Thick Film Resistors are made by screening a layer of resistive glaze onto a ceramic substrate and firing at a temperature above the melting point of the glass frit. Resistance range is controlled by the amount of metal in the glaze and subsequent calibration. A network can be made this way by silk screening the ink (or glaze) in a defined pattern. The cost of the screen preparation is subject to (NRE) charges.

VISHAY PRECISION GROUP

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Design Concepts

Vishay hermetic resistor networks are based on fabrication from a standing inventory of packages and resistor chips. This permits quick delivery of prototypes since there are no masks to design or trial processings to be made. Further, it allows any combination of values, tolerances and circuits. There are normally no engineering or setup charges, and no minimum quantities are required. Delivery can be in two weeks from Vishay's Network Express Prototype Service.

The sequence of fabrication includes selection of chips, die attachment, wirebonding, value trimming, dry nitrogen back-fill, and hermetic sealing. The finished product provides the stability associated with Bulk Metal foil resistors in a hermetically sealed package. Vishay offers a variety of packaging options, as outlined in Table 2 below.

The Available Packages

TABLE 2 - PACKAGES	
DIP, PLUG-IN, LEADLESS CARRIER, AND FLATPACKS	
Ceramic package:	94 % alumina (AL_2O_3)
Lid:	Gold plated Kovar
Attachment:	Solder - tin/gold eutetic
Leads:	Alloy 42 (iron nickel) with 100 µ" gold plating, MIL-STD-1276, type G-21-A
TO packages:	
Metal cover:	Grade A nickel
Header:	Gold plated Kovar
Attachment:	Welded
Leads:	Kovar with 100 µ" gold plating, MIL-STD-1276, type K-21-A
HERMETICITY	
Gross leak:	No bubbles, MIL-STD-202, method 112, test condition D
Fine leak:	< 5 x 10^{-7} cc/s MIL-STD-202, method 112, test condition C, procedure 111A

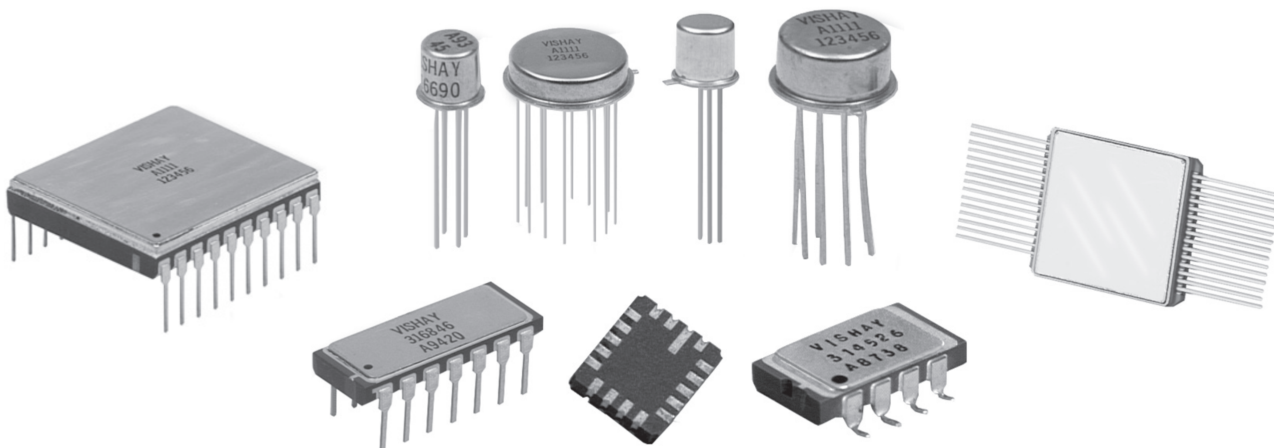

Figure 1. A montage of the packages

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Standard and Custom Packages

- The photo on page 2 shows a broad spectrum of standard network packages available. Selection from one of these standard packages ensures prompt delivery of prototypes.
- Glass-to-metal seal headers offer good thermal dissipation and sharing of temperatures between resistors.
- Ceramic dual-in-line packages offer more pin availability and more chip capacity.
- Ceramic flatpacks offer the lowest profile, but take more board space.
- Ceramic leadless carriers are also available. However, when tight tolerances or low values are considerations, fixturing and associated contact resistance must be taken into account.
- Vishay can develop custom packages for specific applications. Contact our Applications Engineering Department for assistance.

Qualified Producers List

Vishay Models 1445Q and 1446Q networks are qualified to MIL-PRF-83401, Characteristic C, Schematic A. Actual performance exceeds all the requirements of MIL-PRF-83401characteristics “C”.

Model 1445Q contains 7 resistors and 1446Q contains 8 resistors. Qualified resistance range is 100 Ω through 10 kΩ. Other values are available non-QPL. Power rating is 0.1 W per resistor.

Available Circuits

The enclosure method employed by Vishay for DIP, LCC and Flatpack packages utilizes a ceramic package and a gold plated Kovar lid tin/gold solder-sealed to the ceramic. TO packages, have a glass to metal seal header and a metal can or cover is welded to the header. Contact Applications Engineering if special requirements are applicable. See the individual data sheets for package dimensions and chip layout. Table 3 below summarizes the standard packages available.

Hermetic sealing of Vishay's networks enhances their already inherently stable environmental performance. The result is improved load life stability and better performance during high temperature and moisture exposure. Table 1 in “7 Technical Reasons to Specify Bulk Metal Foil Resistor Networks” compares these networks to the requirements of other military types of networks.

TABLE 3 - PACKAGES AND THEIR POTENTIAL CIRCUITS

VISHAY MODEL #	GENERIC PACKAGE	NUMBER OF PINS	CHIP V5x5 CAPACITY	CHIP V15x5 CAPACITY	PACKAGE POWER	EXAMPLES OF CIRCUITS
1401	TO18	3	2	1	0.15 W	Divider, center-tap grounded
1403	TO18	4	5	1	0.15 W	Divider, case grounded
1413	TO5	8	9	3	0.4 W	Divider, case isolated
1417	TO5	8	12	3	0.4 W	Three dividers
1419	TO5	10	12	3	0.4 W	Shift-down weighted ladder
1421	TO8	12	49	16	0.6 W	Four dividers
1422	TO8	16	49	15	0.6 W	7-bit ladder
1442 (1)	DIP	8	12	4	0.4 W	Four feed-through Rs
1445 (1)	DIP	14	30	10	1.2 W	Two decades of BCD ladder
1446 (1)	DIP	16	36	12	1.4 W	11-resistor string with taps
1457	DIP	18	80	25	1.8 W	7-bit R2R ladder
1460	DIP	20	221	73	2.4 W	12-bit R2R ladder
VSM85	LCC	16	12	4	0.4 W	Four dividers
VSM86	LCC	20	16	4	0.6 W	Five dividers
VSM87	LCC	24	16	5	0.6 W	Six dividers
VSM88	LCC	28	25	10	1.0 W	Seven dividers
VSM89	LCC	32	35	14	1.4 W	Eight dividers
1476	Flatpack	30	225	75	2.4 W	12-bit R2R ladder

Note

(1) Available in Gull-Wing Lead-Form package

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Resistor Chips

The principal building blocks of the networks are Vishay Bulk Metal foil resistor chips V5X5, V15X5, and V15X10. Certain speciality chips are also available (or produced on demand) when warranted. Vishay Applications Engineering will assist in determining if a special chip is required. The chips are Bulk Metal foil on high alumina substrate. A protective coating is applied for handling purposes. The pads are gold plated for gold ball bonding interconnects during assembly.

FIGURE 3 - FORMAT OF CHIP RESISTORS USED IN HERMETIC NETWORKS

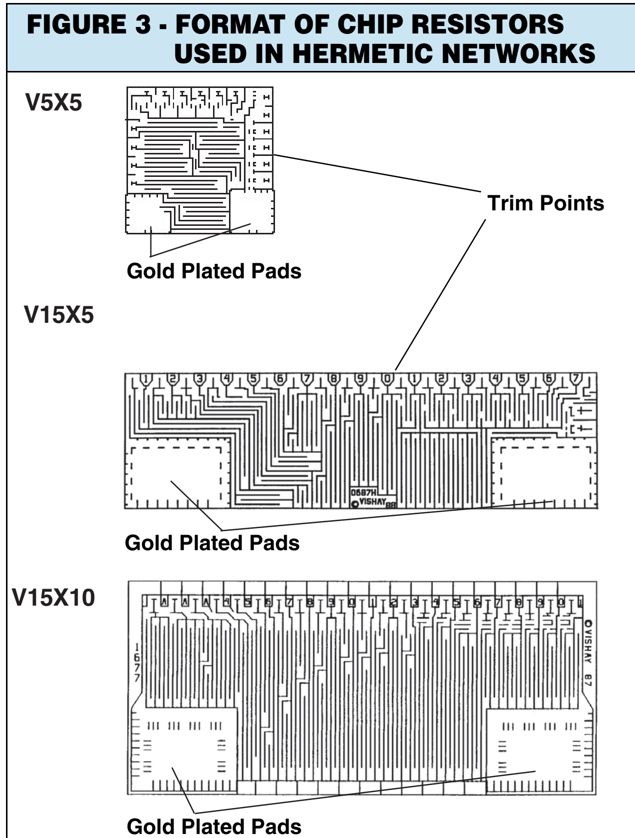


FIGURE 4 - POWER DERATING CURVE

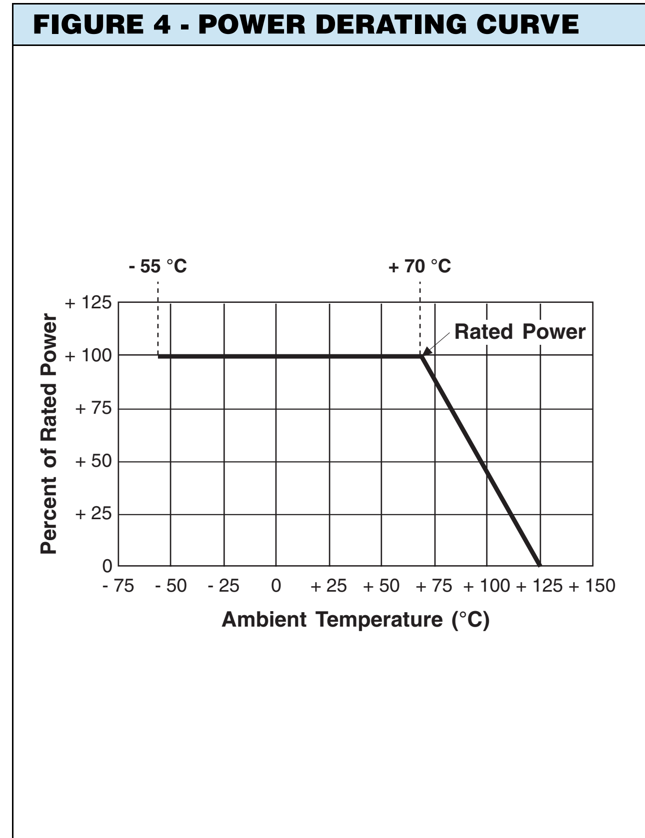
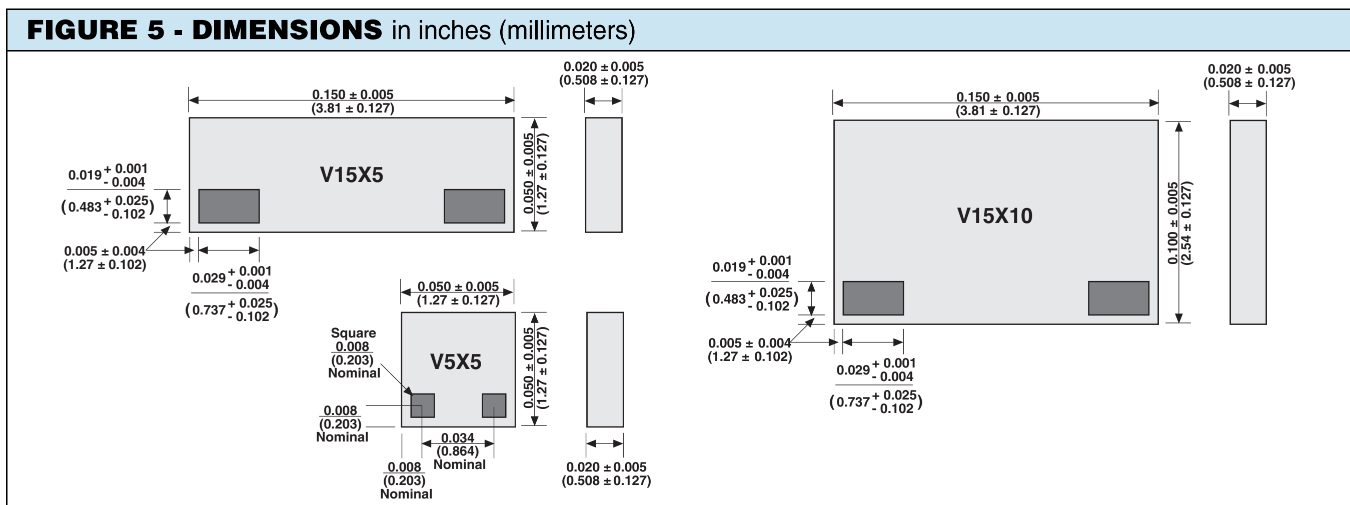


FIGURE 5 - DIMENSIONS in inches (millimeters)



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Quality Inspectioin and Testing

Network performance is established during the engineering design phase and is dependent on the materials of construction. Most characteristics are inherent in the Bulk Metal foil technology and provide the high order of performance displayed throughout this catalog. Stability and drift levels can be improved beyond those shown in the catalog. Applications Engineering is available to recommend screen testing beyond the standard outgoing inspection when catalog limits are insufficient. The chart below shows the standard outgoing testing and the additional user specified screen tests that may be appropriate for a particular application.

Testing of Commercial Product - VISHAY Networks

Our standard outgoing testing consists of:

1. DC resistance test 100 %
   1. 1 Conformity to value
   1. 2 Conformity to tolerance
2. Visual and mechanical 100 %
   2. 1 Conformity to physical size
   2. 2 Cleanliness of leads
   2. 3 Conformity of printing
3. Hermeticity test 100 %
   3. 1 Fine leak test
   3. 2 Gross lead test
4. Shipping inspection (sample plan)
   4. 1 Conformity of packaging
   4. 2 Conformity of count

Additional Testing to MIL Spec

Group A testing to MIL-PRF-83401 imposes the following:

1. Thermal shock 100 %
   5X from - 65 to + 125 °C
2. Power conditioning 100 %
   2. 1 100 h at 25 °C, 1.5 x rated power
   2. 2 ΔR and Δratio calculation
3. Visual and mechanical inspection after the above tests (sample plan)
   3. 1 Conformity to physical size
   3. 2 Workmanship
   3. 3 Damage due to the above tests
4. PDA - 10 % allowed (or one piece, whichever is greater)
5. Solderability (sample plan)

Group B sample testing to MIL-PRF-83401 imposes the following:

1. Temperature coefficient of resistance (sample plan)
2. Resistance to solvents (sample plan)

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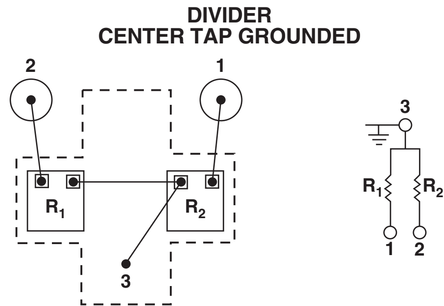
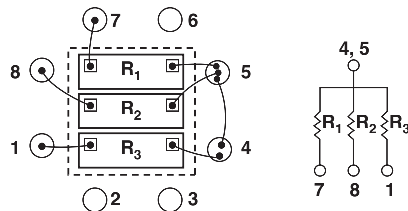
Circuit and Package Examples

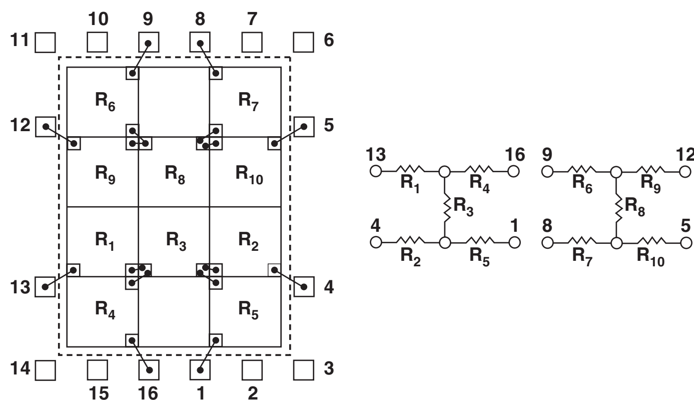
Divider in 1401 package:

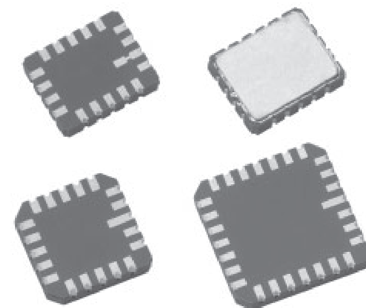


3-resistor array in 1413 package:

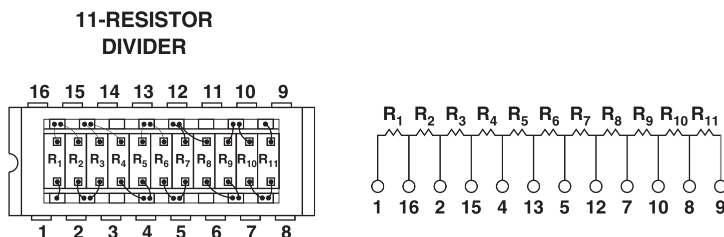


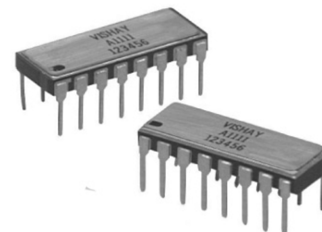
4 voltage dividers in VSM86 package:





11-resistor divider in 1446 package:





For any questions, contact: foil@vishaypg.com